This application is a continuation of U.S. Appl. No. 10/319,599, which is a continuation of U.S. Appl. No. 09/897,601, filed July 3, 2001, which claims the benefit of the following: U.S. Provisional Application No. 60/215,850, filed July 3, 2000; and U.S. Provisional Application No. 60/221,617, filed July 28, 2000, all of which are incorporated herein in their entirety.

***In the Claims*:**

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41. (new) An amplifier array, comprising:

an input node;

a first set of amplifiers, arranged in a parallel fashion, and having their inputs tied together at said input node;

a resistor ladder coupled between said input node and ground; and

a second set of amplifiers, having their inputs tied to corresponding taps on said resistor ladder;

wherein outputs of said first set of amplifiers and outputs of said second set of amplifier are summed together at an output the amplifier array; and

wherein gain for the amplifier array is adjusted by sequentially turning off one or more amplifiers in said second set of amplifiers.

42. (new) The amplifier array of claim 41, further comprising at least one ferrite bead between coupled between said output of the amplifier array and a DC supply.

43. (new) The amplifier array of claim 41, further comprising a capacitor coupled across one or more taps of said resistor ladder.

44. (new) The amplifier array of claim 43, wherein said capacitor flattens the gain of said amplifier array over one or more attenuation settings.

45. (new) The amplifier array of claim 41, further comprising a plurality of capacitors coupled across corresponding taps of said resistor ladder.

46. (new) The amplifier array of claim 41, further comprising a plurality of comparators that correspond to each of said amplifiers in said first set of amplifiers and said second set of amplifiers, wherein each comparator compares a first voltage with a second voltage, resulting in a amplifier control signal that controls said corresponding amplifier in the amplifier array.

47.(new) The amplifier array of claim 46, wherein said control signal turns on said corresponding amplifier when said first voltage is greater than said second voltage.

48. (new) The amplifier array of claim 46, wherein said control signal turns off said corresponding amplifier when said second voltage is greater than said first voltage.

49. (new) The amplifier array of 46, wherein said amplifier control signal causes said corresponding amplifier to operate linearly when a difference between said first voltage and said second voltage is less than a threshold.

50. (new) The amplifier array of claim 46, further comprising a voltage divider having an input that receives an external automatic gain control voltage (AGC) having a voltage range, wherein said voltage divider compresses said voltage range of said AGC voltage to generate said first voltage .

51. (new) The amplifier array of claim 50, wherein said voltage divider includes a means for adjusting compression of said external AGC voltage.

52.(new) The amplifier array of claim 41, wherein said input node is single-ended.

53. (new) The amplifier array of claim 41, wherein said output of the amplifier array is differential.

54. (new) The amplifier array of claim 41, wherein said first set of amplifiers and said second set of amplifiers are fabricated using one or more field effect transistors (FETs).

55. (new) The amplifier array of claim 54, wherein said field effect transistors are fabricated using a CMOS process.

56. (new) The amplifier array of claim 41, wherein said input node is coupled to a diplexer, and said output is coupled to a tuner.

57. (new) The amplifier array of claim 41, further comprising at least one inductor coupled between said output and a DC supply.